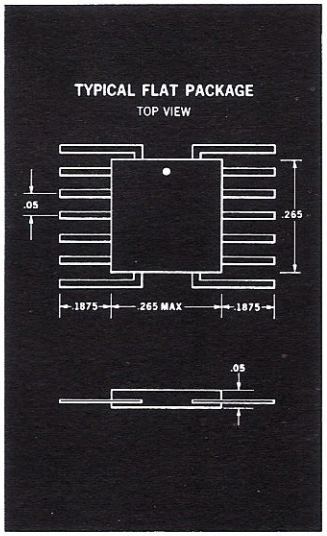
DTμL COMPOSITE DATA SHEET

DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

Diode Transistor Micrologic (DTμL) is the first diode transistor logic circuit expressly designed for integrated circuit technology. As a consequence, DTμL requires only one power supply, which may vary over a wide range without impairing circuit performance. High tolerance to electrical noise, along with ample drive capability is characteristic. Indeed, the designer may exchange one for the other to strike the balance most appropriate to the situation at hand. DTμL is completely characterized and specified over the entire military temperature range of -55°C to +125°C.



CONTENTS OF THIS SPECIFICATION

The optimum operating supply voltage for the full military temperature range is 5.0 volts. The data of this specification enumerated on pages 2 and 3 and the loading rules on page 8 are valid for supply voltages ranging from 4.5 to 5.5 volts. Power dissipation may be reduced by using V_{CC} = 4 V without sacrificing noise immunity or speed if operating temperature is held to a minimum of -20 C, or if fanout is restricted. The Fairchild epitaxial integrated circuit process also permits an operating supply voltage of 6.0 volts over the full temperature range with a slight decrease in fanout or noise immunity at temperatures in excess of 100 C. (See page 8).

For guidance, when designing outside the limits guaranteed by the tests given on pages 2 and 3, graphs of minimum and maximum limits of circuit operation are shown on Pages 6 and 7. These graphs will permit the designer to optimize fanout, noise immunity, supply voltage and temperature for the specific application. Examples using these graphs are given on Page 7.

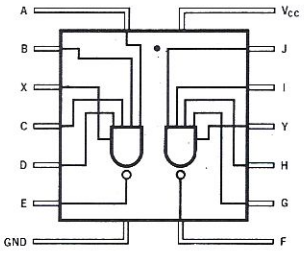
Very extensive noise threshold and propagation delay data are given in the individual DTμL 930 and 931 specification sheets (available on request). Additional propagation delay data is given on Pages 4 and 5 of this specification. Specific characteristics of the Dual Buffer and the Dual Power Gate may be found in the individual DTμL 932 and DTμL 944 specification, while data concerning the effects of input extension appear in the individual DTμL 933 specification.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), -55°C to +125°C, continuous		+8 Volts
Supply Voltage (V_{CC}), pulsed, <1sec		+12 Volts
Output Current, into outputs	DTμL 932, 944	100 mA
Output Current, into outputs	DTμL 930, 931, 946, 962	30 mA

Input Forward Current	-10 mA
Input Reverse Current	1 mA
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

DTμL 930 DUAL GATE
DTμL 932 DUAL BUFFER
DTμL 944 DUAL POWER GATE

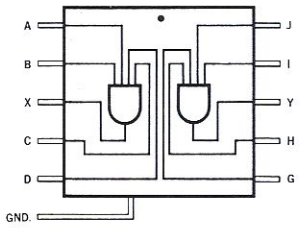


POSITIVE (NAND) LOGIC

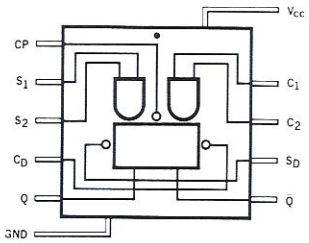
$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

DTμL 933 DUAL EXTENDER



DTμL 931 CLOCKED FLIP-FLOP



J-K MODE TRUTH TABLE

t_n S_2	t_n C_2	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

R-S MODE TRUTH TABLE

t_n S_1	S_2	C_1	C_2	t_{n+1} Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Undetermined

X - Either a one or a zero can be present

"1" more positive than "0"

For J-K Mode Operation:

Connect S_1 to $\overline{Q}$ and C_1 to Q

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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TEST SEQUENCES — DTμL ELEMENTS 930, 931, 932, 933

Abbreviated Test Sequences for the DTμL family of elements are shown below. The ground pin is grounded on all tests. Page 3 of this composite gives a glossary of terms used, tables of test conditions and limits, and LTPD percentages by group.

DTμL 930 & 932 ELEMENTS

NOTE: Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	LIMITS: Sense	Min.	Max.
1, (2)	A		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	V_E (V_F)		V_{OL}
3, 4, 5, 6 (7, 8, 9, 10)	B	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	V_E (V_F)	V_{OH}	
11, (12)	C		V_R	GND	GND	GND			V_{CCH}	I_A I_G		I_R
13, (14)	C		GND	V_R	GND	GND			V_{CCH}	I_B I_H		I_R
15, (16)	C	3	GND	GND	V_R	GND			V_{CCH}	I_C I_J		I_R
17, (18)	C	3	GND	GND	GND	V_R			V_{CCH}	I_D I_J		I_R
19, (20)	D		V_F	V_R	V_R	V_R			V_{CCH}	I_A (I_G)		I_F
21, (22)	D		V_R	V_F	V_R	V_R			V_{CCH}	I_B (I_H)		I_F
23, (24)	D	3	V_R	V_R	V_F	V_R			V_{CCH}	I_C (I_I)		I_F
25, (26)	D	3	V_R	V_R	V_R	V_F			V_{CCH}	I_D (I_J)		I_F
27, (28)	C		GND					V_{CEX}	V_{CEX}	I_E (I_F)		I_{CEX}
29, (30)	B	2	GND					GND	V_{CCH}	I_E (I_F)	I_{SC}	I_{SC}
31	E								V_{PD}	I_{VCC}		I_{PDH}
32	E		GND						V(max)	I_{VCC}		I(max)
33, (34)	E	3					V_X	I_{OH}	V_{CCL}	V_E (V_F)	V_{OH}	
35, 36	F	$t_{pd}+$, $t_{pd}-$ — See table of test circuit conditions and limits, Page 3.										

NOTES: 1. V_{IL} applied individually to 1 input each test. Other inputs open. 2. I_{SC}(max) only for 930; I_{SC}(min) only for 932. ** See LTPD group, Page 5.

3. Delete these tests for 10-pin TO-5 package: 6, 9, 10, 16, 17, 18, 24, 25, 26, 33.

DTμL 931 ELEMENT

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: CP	C_1	C_2	S_1	S_2	C_D	S_D	Q	$\bar{Q}$	V_{CC}	LIMITS: Sense	Min.	Max.
1	C		V_R	GND	GND	GND	GND					V_{CCH}	I_{CP}		I_{RCP}
2, 3, 4, 5	C	1	GND	V_R	V_R	V_R	V_R					V_{CCH}	I_{C1}, I_{C2}, I_{S1}, I_{S2}		I_R
6, 7, 8, 9	D	3		V_F	V_F	V_F	V_F					V_{CCH}	I_{C1}, I_{C2}, I_{S1}, I_{S2}		2/3 I_F
10, 25	D	2	CP, b		V_{IL}		V_{IL}					V_{CCH}	I_{CP}		I_{FCP}
11, 12	B	2	CP, a	V_{IL}	V_{IL}	V_{IH}	V_{IH}			*I_{OH}		V_{CCL}	V_Q	V_{OH}	
13, 14	B	2	CP, a	V_{IH}	V_{IH}	V_{IL}	V_{IL}				*I_{OH}	V_{CCL}	$V_{\bar{Q}}$	V_{OH}	
15	A		CP, c	GND						*	I_{OL}	V_{CCL}	V_Q		V_{OL}
16	A		CP, c			GND				I_{OL}	*	V_{CCL}	$V_{\bar{Q}}$		V_{OL}
17	E		GND	GND	GND	GND	GND					V(max)	I_{VCC}		I(max)
18	E											V_{PD}	I_{VCC}		I_{PDH}
19	B		CP, a			GND	GND	V_{IH}	V_{ILS}	I_{OH}		V_{CCL}	V_Q	V_{OH}	
20	B		CP, a	GND	GND			V_{ILS}	V_{IH}		I_{OH}	V_{CCL}	$V_{\bar{Q}}$	V_{OH}	
21	C		CP, a			GND	GND	V_R				V_{CCH}	I_{CD}		I_R
22	C		CP, a	GND	GND				V_R			V_{CCH}	I_{SD}		I_R
23	D						GND	V_F	GND		GND	V_{CCH}	I_{CD}		I_{FS}
24	D				GND			GND	V_F	GND		V_{CCH}	I_{SD}		I_{FS}
25, 26	F	t_{pd+}, t_{pd-} — See table of test circuit conditions and limits, Page 3.													

NOTES: 1. V_R applied individually to 1 input each test. Other inputs open. 2. V_{IL} applied individually to 1 input each test. Other inputs open. 3. V_F applied individually to 1 input each test. Other inputs open. * Momentary Ground. ** See LTPD group, page 5.

DTμL 933 ELEMENT

Test No.	LTPD** Group	Notes	FORCING CONDITIONS: Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	LIMITS: Sense	Min.	Max.
1, 2, 3, 4 (5, 6, 7, 8)	B	1	GND	GND	GND	GND	I_{FD}	V_X (V_Y)	V_{FD}	V_{FD}
11, (12)	A		V_R	GND	GND	GND		I_A (I_G)		I_R
13, (14)	A		GND	V_R	GND	GND		I_B (I_H)		I_R
15, (16)	A		GND	GND	V_R	GND		I_C (I_I)		I_R
17, (18)	A		GND	GND	GND	V_R		I_D (I_J)		I_R
19, (20)	A						V_R	I_X (I_Y)		5 I_R

NOTE 1. GND applied individually to 1 input each test. Other inputs open. ** See LTPD group, page 5.

GLOSSARY OF TERMS USED WITH DTμL

In General, Subscripts are used as follows:

- O = output
- I = input
- R = reverse, applying to high inputs.
- F = forward, applying to low inputs.
- L = low, applying to a low signal level or when used with V_{CC} to low V_{CC} value.
- H = high, applying to a high-signal level or when used with V_{CC} to high V_{CC} value.

Non-operational Terms:

- V(max) = Maximum rated V_{CC} pin voltage.
- I(max) = Maximum rated current into V_{CC} pin, with V(max) applied.
- V_{PD} = V_{CC} pin voltage applied during power dissipation test.
- I_{PD} = Current into V_{CC} pin with V_{PD} applied. I_{PDL} means gate or buffer inputs are low or 931 clock pin input is low. I_{PDH} means the inputs are high.
- V_R = Input reverse (high) voltage for input diode leakage test.
- I_R = Reverse input diode current with V_R applied to input.
- I_{RCP} = Reverse 931 clock pin input leakage current with V_R applied to input.
- V_{CEX} = Output transistor collector to emitter voltage. With output pull-up resistor connected, $V_{CEX} = V_{CC}$ to avoid drop across output pull-up resistor.

Operational Terms:

- V_{IL} = Input low (threshold) voltage.
- V_{OL} = Output low voltage, with rated fanout current I_{OL} into output.
- I_{CEX} = Output transistor collector to emitter leakage current with V_{CEX} applied to output.
- V_{FD} = Forward diode drop in 933 Element.
- I_{FD} = Forward diode current in 933 Element.
- V_{IH} = Input high (threshold) voltage.
- V_{OH} = Output high voltage, with high output current (I_{OH}) flowing out of output.
- V_F = Forward (low) input voltage, for forward input current (I_F) test. V_F is usually ground.
- I_F = Forward input diode current, for unit input load. Also shown will be 2/3 I_F, I_{FCP}, and I_{FS}.
- I_{OL} = Output low current.
- I_{OH} = Output high current, flowing out of output in V_{OH} test.
- I_{SC} = Short circuit output current to ground, with one or more inputs low. I_{SC} minimum confirms output ability to pull up capacitive loads; I_{SC} maximum confirms subtraction of fanout rules when "OR"ing outputs.
- V_{CCL} = Low V_{CC} pin voltage. Used for V_{OL} (I_{OL}) and V_{OH} (I_{OH}) tests.
- V_{CCH} = High V_{CC} pin voltage. Used for V_{IF} - I_F input forward diode current tests.
- $CP_{,x}$ = Clock Pin, pulsed. The subscript if any refers to pulse waveshape. Used in testing binary elements. (See page 5).
- $V_{CP\,TH}$ = Input Clock Pin threshold voltage (low). With Clock Pin at or below $V_{CP\,TH}$, the 931 "master" Flip-Flop holds the proper "slave" (output) Flip-Flop output high.
- V_X = Input low (threshold) voltage extendable inputs.

TABLE OF CONDITIONS & LIMITS, TPD TESTS (See Test Circuits, Page 5)

(V_{CC} = 5V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	930	3.9 K	30 pf	25 nsec	80 nsec
t_{pd-}	930	400 Ω	50 pf	10 nsec	30 nsec
t_{pd+}	932	510 Ω	500 pf	25 nsec	80 nsec
t_{pd-}	932	150 Ω	500 pf	15 nsec	40 nsec
t_{pd+}	930	400 Ω	50 pf	15 nsec	40 nsec[1]
t_{pd-}	930	3.9 K	20 pf	5 nsec	20 nsec[1]
t_{pd+}	932	150 Ω	500 pf	20 nsec	65 nsec[1]
t_{pd-}	932	510 Ω	200 pf	8 nsec	30 nsec[1]

(V_{CC} = 5V, T = 25°C)

		R	C_2	Min.	Max.
t_{pd+}	931	3.9 K	30 pf	35 nsec	75 nsec
t_{pd-}	931	400 Ω	30 pf	35 nsec	75 nsec
t_{pd+}	931	400 Ω	30 pf	20 nsec	50 nsec[1]
t_{pd-}	931	3.9 K	30 pf	30 nsec	70 nsec[1]

NOTE 1: Correlating limit provided as design information only.

TABLE OF TEST LIMITS

		Units	-55°C Min.	-55°C Max.	+25°C Min.	+25°C Max.	+125°C Min.	+125°C Max.
V_{OL}		Volts		.40		.40		.45
V_{OH}		Volts	2.5		2.6		2.5	
I_R		μA		2.0		2.0		5.0
I_{RCP}		μA		20.0		20.0		30.0
1 I_F		mA		-1.60		-1.60		-1.50
2/3 I_F		mA		-1.07		-1.07		-1.00
I_{FCP}		mA		-3.4		-3.40		-3.00
I_{CEX}		μA				50.0		
I_{SC}	930	mA		-1.34	-.60	-1.34		-1.30
I_{SC}(min)	932	mA	-16.		-18.		-16.	
V_{FD}		Volts	.85	.98	.70	.82	.50	.65
I(max)	930	mA				5.50		
I(max)	931	mA				14.5		
I(max)	932	mA				6.0		
I_{PDH}	930	mA				6.50		
I_{PDH}	931	mA				11.0		
I_{PDH}	932	mA				26.6		
5 I_R		μA		10.0		10.0		25.
I_{FS}		mA		-1.20		-1.20		-1.10

TABLE OF FORCING CONDITIONS

	Units	-55°C	+25°C	+125°C		Units	-55°C	+25°C	+125°C		Units	-55°C	+25°C	+125°C
V(max)	Volts	--	8	--	V_{CEX}	Volts		4.5		I_{OL} 932	mA	34	36	32
V_{PD}	Volts	--	5	--	I_{OH}	mA	-.12	-.12	-.12	I_{OH} 932	mA	-2.0	-2.5	-4.0
V_{CCH}	Volts	5.5	5.5	5.5	I_{OL} 930	mA	11.4	12.0	10.8	V_{IL}	Volts	1.4	1.10	.80
V_{CCL}	Volts	4.5	4.5	4.5	I_{FD}	mA	2	2	2	V_{IH}	Volts	2.1	1.9	1.7
V_R	Volts	4.0	4.0	4.0	V_{ILS}	Volts	1.40	1.10	.80	$V_{CP\,TH}$	Volts	1.10	.95	.75
V_F	Volts	0	0	0	I_{OL} 931	mA	10.0	10.6	9.5	V_X	Volts		1.80	

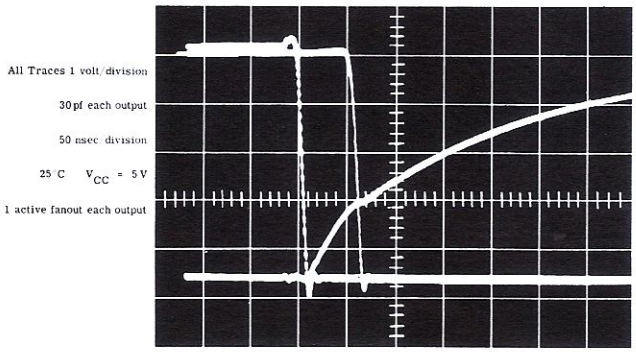
ADDITIONAL DELAY TIME CHARACTERIZATION INTO CAPACITIVE LOADS

The individual specifications on DTμL 930 and DTμL 931 give extensive delay characterizations as functions of V_{CC}, temperature, fanout and ratio of active to inactive fanout. For each fanout, active or inactive, 5 pf wiring capacity was added. This page will show the effects of greater wiring capacities.

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output, as shown in the pictures below. In the 1st time period, from the saturated low level to threshold, the R of the R-C time constant can be given by 6 KΩ in parallel with $\frac{3.75\,K\Omega}{\text{active fanout}}$. Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R-C time constant is 6 KΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level; so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. DTμL 930, 932, 933, and 931 inputs (except CP) are ~ 2 pf per input for active or inactive fanout; the remaining capacitance is from board, wiring, and connectors.

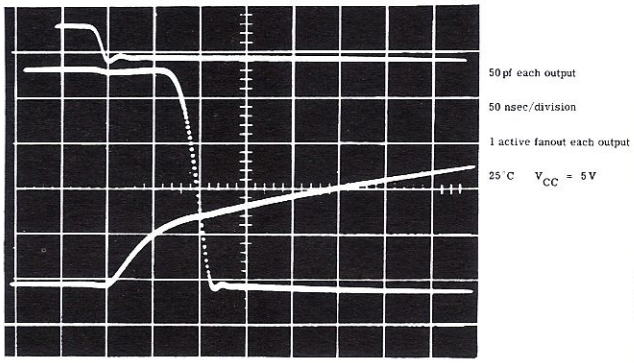
The t_{pd} average curves, with 1 active fanout, Fig. 1 below, and the typical maximum toggling frequency curve, Fig. 2, give the prediction of capacitive effects on switching speeds. For frequency division or ripple carry counting, use of 3 KΩ external resistors tied from output to V_{CC} in the least significant bit will increase the maximum frequency. In Fig. 1 each output has 1 active fanout, which is worst case.

DTuL 930 — INVERTER PAIR DELAY



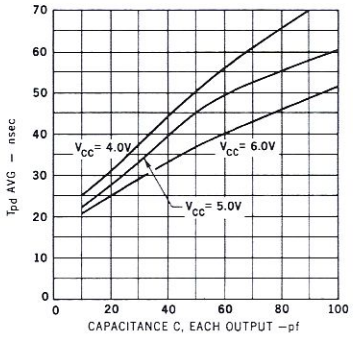
1st Negative Going Trace - Input to 1st Gate
Positive Going Trace - Output of 1st Gate = Input to 2nd Gate
2nd Negative Going Trace - Output of 2nd Gate

DTuL 931 — DIVIDING BY 2



Upper Trace - Input to CP (5 volts/division)
Positive Going Trace - Output Going High (1 volt/division)
Negative Going Trace - Output Going Low (which starts Going low as the positive Going Trace reaches threshold) (1 volt/division).

FIG. 1
T_{pd} AVERAGE VS. CAPACITY
(DTμL 930, 25°C)



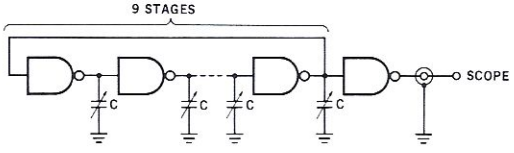
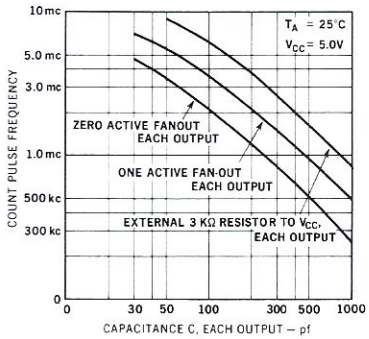
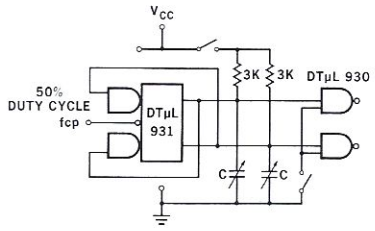


FIG. 2
TYPICAL MAXIMUM BINARY COUNTING RATE VS. CAPACITY





DTμL 930 TIME DELAYS VS. CAPACITIVE LOADS

FIG. 3

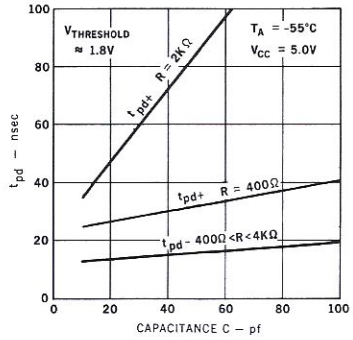


FIG. 4

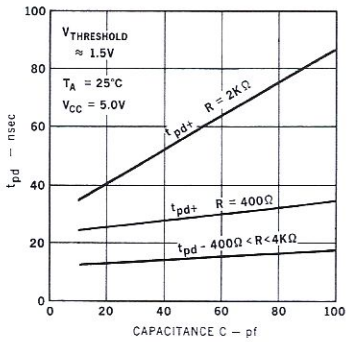
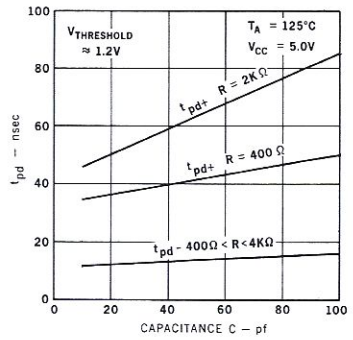
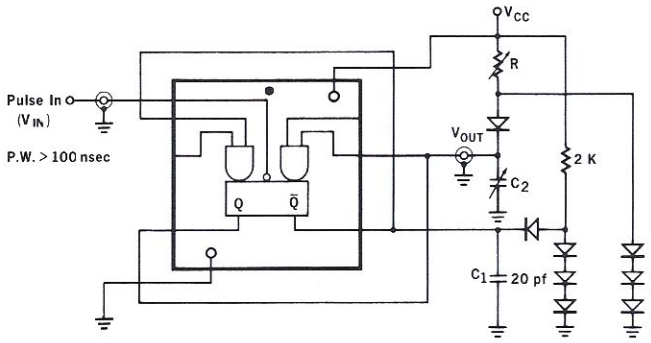


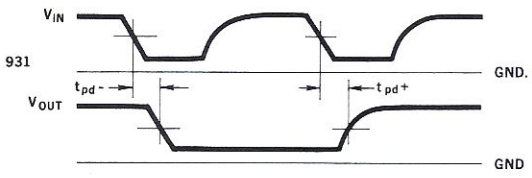
FIG. 5



t_{pd} test circuit for 930 & 932 used (see below)

Tpd TEST CIRCUIT DTuL 931

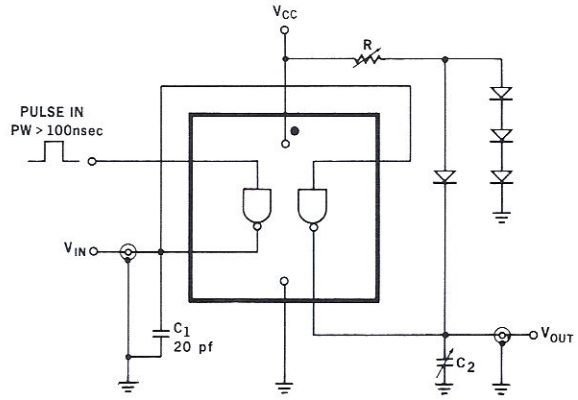


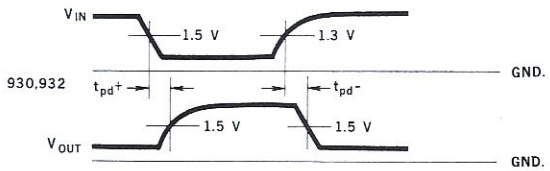


C_1 and C_2 includes probe and jig capacitance

$V_{Threshold}$ = 1.5 V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

Tpd TEST CIRCUIT DTuL 930, 932





T_{pd} - of 930, 932, and 946 elements will be read from input at 1.3 V.

All diodes FD600 or equivalent.

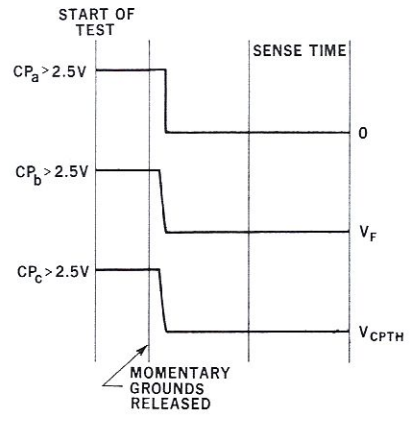
TABLE OF LTPD's

(These apply to the test sequence on page 2)

Group	-55°C	+25°C	+125°C
A	15%	10%	15%
B	-	10%	15%
C	-	10%	15%
D	-	10%	15%
E	-	10%	15%
F	-	10%	-

CLOCK PIN WAVEFORMS

(For 931 Test Sequence, Page 2)



MINIMUM-MAXIMUM DC CURVES I_F VS. V_F & V_{CC}

FIG. 1
$-1\ I_F$ DTμL 930, 932, 944, 946, 962
MAXIMUM VS. TYPICAL
($V_F = 0V$ & $V_F = .750V$ $T_A = -55°C$ & $+25°C$)

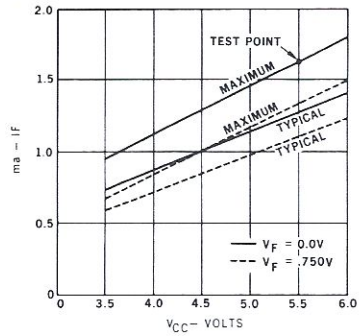
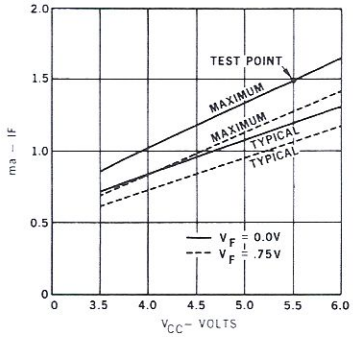


FIG. 2
$-1\ I_F$ DTμL 930, 932, 944, 946, 962
MAXIMUM VS. TYPICAL
($V_F = 0V$ & $V_F = .750V$ $T_A = +125°C$)



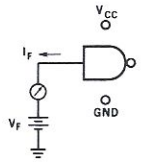
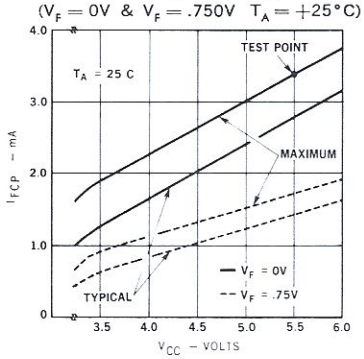
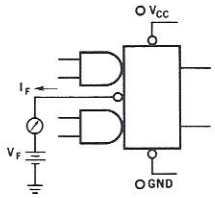


FIG. 3
I_{FCP} DTμL 931
MAXIMUM VS. TYPICAL
($V_F = 0V$ & $V_F = .750V$ $T_A = +25°C$)



Note that with $V_F = 0$ and Inputs S_1, S_2, C_1, and C_2 at V_{OL}, I_{FCP} current is summed through three diodes—both input AND Gate diodes and one of the Clock-coupling transistor emitters. As the Clock Pin voltage (V_F) rises to approach V_{OL}, current starts to flow into one of pins S_1, S_2, C_1, or C_2 (since all of these pins high is not an allowed logic state). Also when the collector of the Clock-coupling transistor rises (the collector is at $V_{CE}(sat) + V_F$), current flows into the low output of the cross-connected output Flip-Flop. Therefore, I_{FCP} equal to 2 I_F is a conservative rating and test current is much higher than will flow "in use."



OUTPUT LOW CURRENT VS. V_{CC} OR V_{OL} FOR 930 AND 931 ELEMENTS

FIG. 4
I_{OL} VS. V_{CC}
($T_A = +25°C$, $V_{OL} = .400V$)

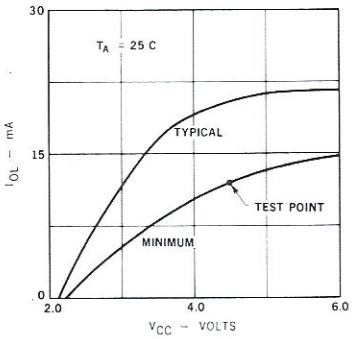


FIG. 5
I_{OL} VS. V_{CC}
($T_A = -55°C$, $V_{OL} = .400V$)

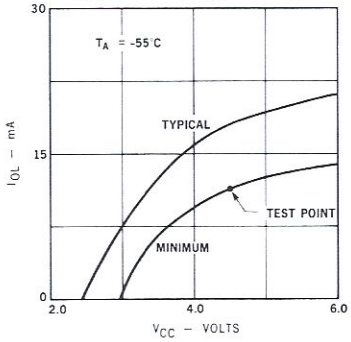
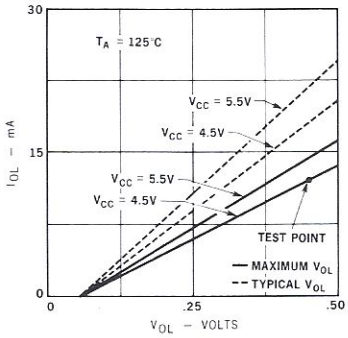
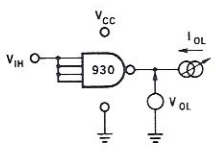
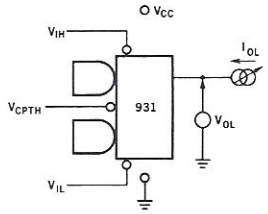


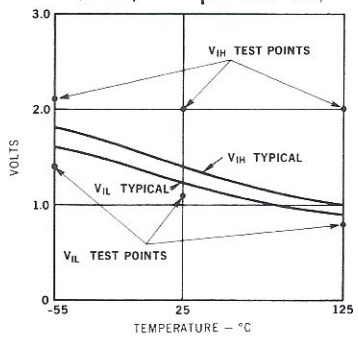
FIG. 6
I_{OL} VS. V_{OL} VS. V_{CC}
TYPICAL VS. MAXIMUM ($T_A = +125°C$)



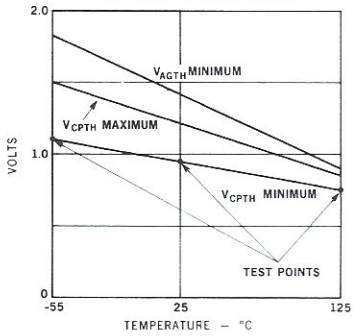




DT μL INPUT THRESHOLDS VS. TEMPERATURE (except DT μL 931 CP)



DT μL CLOCK PIN THRESHOLDS VS. TEMPERATURE



DEFINITIONS OF 931 CLOCK PIN THRESHOLDS

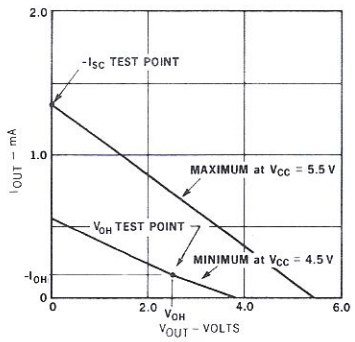
$V_{AG\,TH}$(min) With CP at or above $V_{AG\,TH}$(min), the clocked inputs will control the state of the "master" Flip-Flop, with V_{CC} and clocked -inputs worst case.

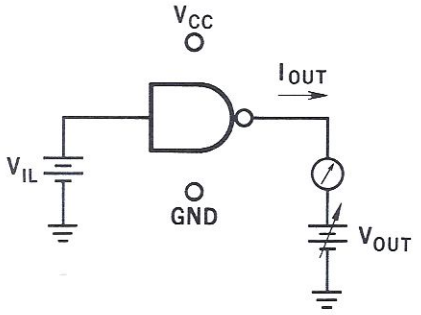
$V_{CP\,TH}$(min) With CP at or below $V_{CP\,TH}$(min), the "master" Flip-Flop will control the output Flip-Flop, with V_{CC} and outputs worst case.

$V_{CP\,TH}$(max) With CP at or above $V_{CP\,TH}$(max), the "master" Flip-Flop will not control the output Flip-Flop, with V_{CC} and outputs worst case.

OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR DTμL 930 AND 931 ELEMENTS

FIG. 9

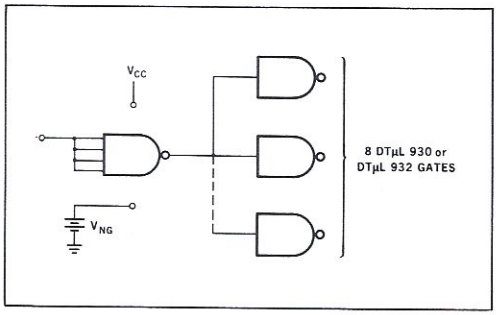




EXAMPLES OF USES FOR THE MINIMUM–MAXIMUM DC CURVES (Pages 6 & 7)

EXAMPLE 1.

A low DTμL 930 output at -55°C fans out to 8 inputs of DTμL 930 or 932. V_{CC} = 5 V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 930. Its output may thus rise to .75 Volt (V_{NG} + V_{OL}). 4.65 Volts (V_{CC} - V_{NG}) remain from V_{CC} pin to ground pin; this is above V_{CCL} = 4.50 V, and test I_{OL} is conservative. Maximum current flowing in each input of the 8 930/932's is given by Fig. 1 on Page 4 with V_F = 0.75 V and V_{CC} = 5 V; the current (I_F) is less than 1.25 mA and total current ($\leq$8 x 1.25 = 10 mA) is less than the I_{OL} test current used at -55°C to saturate the low output. Above the 350 mV of V_{NG} already applied, the difference between the common node voltage ($\leq$.75 V) and the low input threshold (V_{IL} = 1.40 V) of the 8 930/932's is still $\geq$350 mV, allowing for signal noise to be superposed above ground noise.



EXAMPLE 2.

The I_F and I_{OL} curves on Page 6 may be expressed in analytical form, as follows

$$I_F \text{ (930 and 932)} \leq \frac{V_{CC} - V_F - V_{FD}}{3\,K\Omega} \quad T_A < 25°C$$

For T_A greater than 25°C, the 3 KΩ rises by 0.12%/°C to approximately 3.36 KΩ at +125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.70 V at 25°C and 1 mA. $\Delta V_{FD}/°C$ is roughly 1.8 mV/°C.

The ratio of I_{OL}, on 930 and 931 (Figs. 4, 5, and 6) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL} \text{ @ } -55°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} \geq \frac{V_{CC} - 3.0\,V}{4.5\,V - 3.0\,V}$$

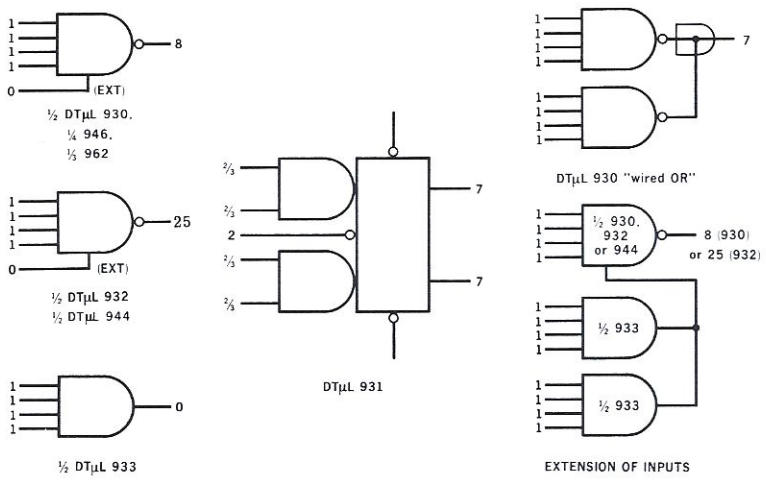
and by

$$\frac{I_{OL} \text{ @ } 25°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} \geq \frac{V_{CC} - 2.3\,V}{4.5\,V - 2.3\,V}$$

Since, at 25°C, $I_{OL} \geq$ 12 mA at V_{CCL} = 4.5 V is guaranteed by the Page 2 and 3 specifications, I_{OL} at V_{CC} pin to GND pin voltage of 3.6 V is $\left(\frac{3.6 - 2.3}{4.5 - 2.3}\right)$12 mA = 7.1 mA.

The similar expression for the 932 gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive $\left(\frac{V_{OL}}{I_{OL}} \text{ saturation resistance}\right)$ slope. Fig. 6 at +125°C shows this, with V_{CC} having relatively small effect.

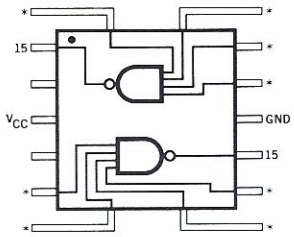
SUGGESTED INPUT—OUTPUT LOADING FACTORS



The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

RULES FOR USE OF TTμL 103 AND 104 WITH DTμL

($4V < V_{CC} < 6V$)



* = 2 input loads for fan-in = 1 to DTμL output driver.
* = 3 input loads for fan-in ≥ 2 to DTμL output driver.
* = 1 input load to TTμL output driver.

These input loads are primarily determined by inverse beta leakage at the TTμL inputs at +125°C. For special cases where improved loading rules may be required, please consult the Fairchild Sales representative.

The TTμL makes an excellent output interface driver for DTμL. TTμL outputs can be tied thru external loads to 8 or 10 V separate voltage supplies, to obtain output levels up to 6 or 8 volts.

MISCELLANEOUS RULES

1. Outputs of DTμL 930 may be tied together for the "wired OR" function $(\overline{ABCD} \cdot \overline{GHIJ} = \overline{ABCD + GHIJ})$. Subtract 1 unit fanout for each added gate. Subtract 5 fanouts for six added gates.

2. Outputs of DTμL 932 may not be tied together for the "wired OR" function.

3. Extension of inputs with the DTμL 933 does not affect quiescent loading of the supplemented element (DTμL 930 or 932). However, capacitance due to wiring to the DTμL 933 will affect noise tolerance and propagation delay, and thus establish a fanin limit for the particular application. Please refer to the typical curves on the DTμL 933 Dual Extender Element preliminary specifications.

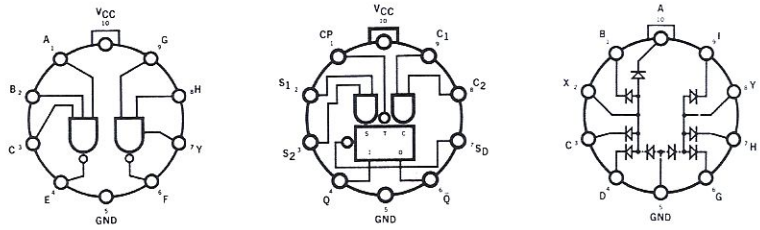
4. For operation with a nominal supply voltage of 4.0 volts from -55°C to +125°C, reduce element fanout as follows: DTμL 930 = 5, DTμL 931 = 5, DTμL 932 = 18. If temperature is maintained above -20°C, no fanout reduction is necessary.

5. For operation with a nominal supply voltage of 6.0 volts from -55°C to +125°C, reduce element fanout as follows: DTμL 930 = 6, DTμL 931 = 6, DTμL 932 = 20. If ambient temperature remains below +100°C or if worst case Noise Threshold is considered to be 250 mV, no fanout reduction is necessary.

Except as noted, these rules apply over the entire military temperature range with a supply voltage of 4.5 to 5.5 volts. These rules also permit a 50°C temperature differential between individual elements. These rules guarantee a worst case signal-line or ground Noise Threshold of at least 350 mV. Practical Noise Thresholds exceed 500 mV.

6. All rules for DTμL 930 apply to DTμL 946 and DTμL 962.

10 LEAD TO—5 PACKAGE PIN LOCATIONS



DTμL 930 DUAL GATE
DTμL 932 DUAL BUFFER
DTμL 944 DUAL POWER GATE

DTμL 931
CLOCKED FLIP-FLOP

DTμL 933
DUAL EXTENDER

PURCHASING INFORMATION

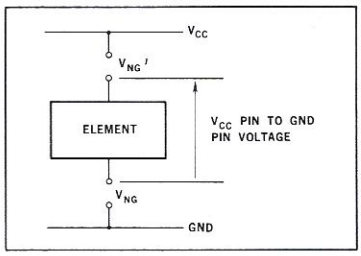
9YXXX5Z

Y = 1 for 14 pin CERPAK
Y = 5 for 10 pin TO-5
XXX = 930
931
932
933
Z = 1 for -55°C to +125°C operation

(cont'd)

EXAMPLE 3.

The test sequences on Page 2 and tables of conditions and limits on Page 3 use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC}, for example, and assuming $\Delta V_{CC} = \pm .2$ V, testing at $V_{CCL} = 4.5$ V and $V_{CCH} = 5.5$ V allows simulation of ± 0.3V ground noise V_{NG} or V_{CC} line noise V_{NG}'. Since there is gain associated with V_{NG} (refer to DTμL 930 and 931 specifications), particularly at lower temperatures and V_{CC} values; the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F = V_{OL}$, the worst case low output level, or even into $V_F = V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Page 6 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fanout, power, and noise margin tradeoffs for this unique application.



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